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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/030,252	01/09/2002	Tetsuro Yoshimoto	60188-141	1962

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EXAMINER	
KOYAMA, KUMIKO C	
ART UNIT	PAPER NUMBER
2876	

DATE MAILED: 03/23/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/030,252	YOSHIMOTO ET AL.	
	Examiner	Art Unit	
	Kumiko C. Koyama	2876	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *27 December 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-16* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *14* is/are allowed.

6)☒ Claim(s) *1,2,4-13,15 and 16* is/are rejected.

7)☒ Claim(s) *3* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *09 January 2002* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *122704*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Acknowledgement is made of receipt of Amendment filed on December 27, 2004/

Claim Objections

1. Claims 1-16 are objected to because of the following informalities:

The Examiner respectfully requests the Applicant to avoid the use of "/" because it renders the claim indefinite since it is unclear whether "/" is considered as an "or" or "and." For Examination purposes, all the "/" are considered as "or." For example, "sends/receives" are considered as "sends or receives." However, the Examiner respectfully requests the Applicant that "sends/receives" to be changed to --sends or receives-- as well as remaining of the phrases with slashes.

Appropriate correction is required.

Claim Rejections - 35 USC § 103

2. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

3. Claims 1-2 and 9-13 are rejected under 35 U.S.C. 103(a) as being unpatentable over Asami (US 6,036,100) in view of Dreifus (US 4,575,621) and Kakiage et al (US 5,968,166).

Re claims 1, 9 and 13: Asami teaches a noncontact IC card that transmits and receives data to and from a host computer using RF signals (col 3, lines 27-36). The IC card includes a rectification circuit that rectifies the RF signal received by transmission antenna unit to supply current to the other internal components of IC card and the rectification circuit thus acts as a power supply unit for the internal circuitry of IC card (col 1, lines 29-34). The IC card is supplied with a power from the outside in a contactless manner because the rectification circuit provides power to the IC card when there is an RF signal, which is from outside and considered as a power supply, received by transmission antenna. Asami also teaches that the noncontact IC card includes a Trans/Receipt antenna unit 3, a buffer memory 10 and EEPROM 7 (nonvolatile memory). The noncontact IC card further includes an UART for transmitting data received by the antenna unit 3 and a modulation circuit 4/demodulation circuit 5 to the buffer memory 10 and transmitting data stored in the buffer memory 10 to the antenna unit 3 and therefore, the UART acts as the DMA circuit (col 3, lines 27-36, col 4, lines 27-45). The control circuit 8 acts both a CPU and a state control means. It acts as a CPU because the control circuit 8 executes write/read process on the buffer memory 10 and the EEPROM 7 by setting the enable signal for the data processing (col 4, lines 32-40, 55-60). The control circuit 8 is also considered as a state control means because it halts or does not processes the operation of the EEPROM/nonvoatile memory while the antenna unit is transmitting or sending data to/from the outside (col 4, lines 55+, Fig 2, and Abstract). The control circuit 8 also halts or disables its own operation to the EEPROM/nonvolatile memory, which is also considered as halting the operation of the CPU.

Asami fails to teach that the IC card comprises a DMA circuit.

Dreifus teaches a portable electronic transaction device including means for transmitting and receiving information to and from the terminal (col 3, lines 20-21), and an integrated circuit means 6 (col 6, lines 24-25) that has a communication buffer 64, direct memory access (DMA), read only memory (ROM), central processing unit (CPU) and an interrupt control unit circuit 62 (col 8, lines 20-27). Dreifus discloses that since the direct memory access (DMA) circuit 60 is connected to the RAM and to the interrupt control circuit 62 and since the interrupt control circuit is in turn connected to the time/date clock 66 and the communication buffer 64, DMA circuit 60 allows the RAM 58 to receive information directly from the time/date clock 66 and to transmit and receive the data from the terminal 20, via the communication buffer and the interrupt control unit 62, without relying on the operation of the central processing unit (col 9, lines 1-16).

Therefore, it would have been obvious to an artisan of ordinary skill in the art at the time the invention was made to integrate the teachings of Asami to the teachings of Dreifus in order to rapidly process the data received so that there are enough space to be utilized and process the data to be transmitted so that constant data transmission can be maintained for faster transmission.

Asami as modified by Dreifus fail to teach halting the write/read processing on the buffer memory and the nonvolatile memory of the CPU while the transmission circuit is sending/receiving data to/from the outside.

Kakiage discloses that when the data read from the external memory 150 has not yet been written in the read buffer data register 9, the control circuit 4 requests the CPU 120 to halt execution of the read instruction by pausing the assertion of the response signal 113 and waits

until the data read from the external memory 150 is written into the read buffer data register 9. When the necessary data is written into the read buffer 9, the control circuit 4 asserts the response signal 113 to release the CPU 120 from the halt state and transfers the data to the CPU 120 (col 17, lines 30-40).

Therefore, it would have been obvious to an artisan of ordinary skill in the art at the time the invention was made to integrate the teachings of Kakiage to the teachings of Asami as modified by Dreifus such that the read operation is not constantly operating when there is no data to be read, and utilizes less power and increases productivity by providing such control to the read operation.

Re claim 2: Fig. 9 shows an interruption signal (c) that occurs between the 1st and 2nd data bit (m bytes) that enables data processing.

Re claim 10: The control circuit unit 8 functions as both a central processing unit and a state control as described above. The data processing, which is central processing, is disabled, or in other words halted, while the data receive signal is enabled (col 4, lines 55+). When the data receive signal is enabled, the data signal is received from the host apparatus 2 and stored at buffer 10 via the UART (col 3, lines 44-54). The UART is modified and replaced by a DMA circuit as shown in the combination of Asami in view of Dreifus as provided above in claim 1.

Re claim 11: The control circuit unit 8 functions as both a central processing unit and a state control as described above. The data processing, which is central processing, is disabled, or in other words halted, while the data receive signal is enabled (col 4, lines 55+). However, the state controls of the control circuit unit 8 is still in an operative state by setting the enable and disable signals to control the states (col 4, lines 55+).

Re claim 12: Asami discloses that if no data is received after the data received period, the data processing enable signal (c) is set HIGH, and the data stored in the buffer 10 is processed (col 5, lines 5-10).

4. Claims 4 and 5 are rejected under 35 U.S.C. 103(a) as being unpatentable over Asami in view of Dreifus and Kakiage as applied to claim 1 above, and further in view of the admitted prior art. The teachings of Asami as modified by Dreifus and Kakiage have been discussed above.

Asami teaches that the antenna unit and the modulating circuit work together in a sequential manner and therefore, is considered as a transmission circuit as a whole. As shown in Fig. 2, the signal (c) shows that a signal that is set HIGH to enable processing of the data other than the times when the data is being transmitted, which is represented by signal (a). A preset signal is inherently taught because it is necessary to provide some type of electrical signal in order to set the signal HIGH.

Asami as modified by Dreifus and Kakiage fails to teach that the data received by the transmission circuit has a structure in accordance with the standard of ISO-IEC 14443-3.

The admitted prior art discloses the ISO 14443-3 in the Background Art section of the application and the standard ISO 14443-3 was known by others before the applicant's invention. Furthermore, the it discloses that "contactless IC cards under development in various companies are to comply with the anti-collision function of ISO 14443-3 for allowing one reader/writer to simultaneously write/read data in/from a plurality of IC cards."

Therefore, it would have been obvious to an artisan of ordinary skill in the art at the time the invention was made to modify the teachings of Asami as modified by Dreifus and Kakiage

and have an IC card that is compliant to 14443-3 in order to transfer data to multiple IC cards without having erroneous data transfer.

5. Claim 6 is rejected under 35 U.S.C. 103(a) as being unpatentable over Asami in view of Dreifus and Kakiage as applied to claim 1 above, and further in view Arai (US 5,845,134). The teachings of Asami as modified by Dreifus and Kakiage have been discussed above.

Asami as modified by Dreifus and Kakiage fail to teach an IC card comprising a resume circuit for storing, when data write processing on the nonvolatile memory executed by the CPU is interrupted, a proceeding state of the write processing up to time of interruption, wherein the CPU resumes the write processing on the nonvolatile memory on the basis of the proceeding state stored in the resume circuit.

Arai teaches a resume control system of a computer system having a CPU provided with a system management mode for accessing a predetermined memory space and a protect mode with a memory addressing method different from the system management mode (col 14 lines 40-44). Arai also teaches a first resume means for executing first resume processing for restoring the status data of the computer system and system management means for managing an operation of the computer system.

Therefore, it would have been obvious to an artisan of ordinary skill in the art at the time the invention was made to integrate the teachings of Arai to the teachings of Asami as modified by Dreifus and Kakiage in order to avoid the writing process while data transmission to avoid error in transmission and continue when the transmission of data is over so that the system is not remain paused, but to start up the process again, which utilizes the time efficiently without wasting time.

6. Claims 7 and 8 are rejected under 35 U.S.C. 103(a) as being unpatentable over Asami in view of Dreifus and Kakiage as applied to claim 1 above, and further in view of Yamaguchi (US 5,365,047). The teachings of Asami as modified by Dreifus and Kakiage have been discussed above.

Asami as modified by Dreifus and Kakiage fail to teach wherein the state control circuit includes a time counting circuit for starting counting time in response to the CPU going into halt state, stopping counting the time in response to restoration of the CPU to an operative state and outputting a counted value to the CPU. Asami also fail to teach a time monitoring circuit for starting counting time in response to the CPU going into a halt state and outputting a timeout signal to the CPU when the CPU does not restore to an operative state before a counted value reaches a given value and wherein the CPU goes into the operative state in response to the timeout signal output by the time monitoring circuit.

Yamaguchi teaches an IC card comprising a timer means for counting a set time (col 3, lines 5-16).

Therefore, it would have been obvious to an artisan of ordinary sill in the art at the time the invention was made to modify the teachings of Yamaguchi to the teachings of Asami as modified by Dreifus and Kakiage in order to ensure that the data are transmitted at a proper rate as well as within a certain amount of time so that when data transmission is not complete within a certain amount of time, the card can acknowledge that the transmitted data may contain erroneous data, and thereby preventing erroneous data to be stored in the IC card.

Response to Arguments

7. Applicant's arguments with respect to claims 1-13 and 15-16 have been considered but are moot in view of the new ground(s) of rejection.

Applicant has amended new limitation to the claims, such as "the write/read processing on said buffer memory and said nonvolatile memory." Such new limitation necessitated new search and consideration. New grounds of rejection have been applied.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Kumiko C. Koyama whose telephone number is 571-272-2394. The examiner can normally be reached on Monday-Friday 8am-4:30pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Michael G. Lee can be reached on 571-272-2398. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Kumiko C. Koyama

Kumiko C. Koyama

March 19, 2005

DIANE I. LEE
PRIMARY EXAMINER